In the Claims:

Please amend claims 22, 23, 30, 32 and 33. The status of the claims is as follows:

1-21. (Canceled)

22. (Currently Amended) A method of manufacturing an image display apparatus including an image display unit with a plurality of pixels arranged in a matrix, a first control circuit for controlling the drive of rows of said image display unit, and a second control circuit for controlling the drive of columns of said image display unit, at least one of said image display unit and said first and second control circuits including a plurality of CMOS transistors each of which comprise p- and n- type thin film transistors and which ~~have~~ are classified into at least two element groups having different operating voltages, said method of comprising the steps of:

non-selectively doping a thin film with p-type impurities, said thin film to be an active semiconductor layer including first prospective regions to form p-type thin film transistors and second prospective regions to form n-type thin film transistors;

selectively doping only said second prospective regions of said thin film with p-type impurities at a higher concentration than that in said step of non-selectively doping; and

annealing said thin film to activate the p-type impurities contained therein,

wherein each of said CMOS transistors is subjected to a predetermined number

of times of said step of non-selectively doping necessary for the CMOS transistor and a predetermined number of times of said step of selectively doping necessary for the CMOS transistor so that threshold voltages of the p-and n-type thin film transistors ~~constituting~~ included in the CMOS transistor are independently set in accordance with the operating voltage of the CMOS transistor.

23. (Currently Amended) A method of manufacturing an image display apparatus including an image display unit with a plurality of pixels arranged in a matrix, a first control circuit for controlling the drive of rows of said image display unit, and a second control circuit for controlling the drive of columns of said image display unit, at least one of said image display unit and said first and second control circuits including a plurality of CMOS transistors each of which comprises p- and n-type thin film transistors and which ~~have~~ are classified into at least two element groups having different operating voltages, said method comprising the steps of:

non-selectively doping a thin film with p-type impurities, said thin film to be and active semiconductor layer including first prospective regions to form p-type thin film transistors and second prospective regions to form n-type thin film transistors;

selectively doping only said second prospective regions of said thin film with p-type impurities at a higher concentration than that in said step of non-selectively doping; and

annealing said thin film to activate the p-type impurities contained therein,

wherein ~~each of part of~~ some among said CMOS transistors ~~is~~ are subjected to a predetermined number of times of said step of non-selectively doping necessary for the CMOS ~~transistor~~ transistors and a predetermined number of times of said step of selectively doping necessary for the CMOS ~~transistor~~ transistors, and ~~each of the~~ other ~~part of~~ said CMOS transistors ~~is~~ are subjected to only a predetermined number of times of said step of non-selectively doping necessary for the CMOS ~~transistor~~ transistors, so that threshold voltages of the p- and n- type thin film transistors ~~constituting~~ included in each of said CMOS transistors are independently set in accordance with the operating voltage of the CMOS transistor.

24. (Original) A method according to claim 23, wherein said image display unit has liquid crystal cells as said pixels and CMOS transistors with a high operating voltage, and

said first control circuit comprises a low-voltage operation unit having CMOS transistors with a relatively low operating voltage and a high-voltage operation unit having CMOS transistors with a high operating voltage.

25 (Original) A method according to claim 23, wherein said step of non-selectively doping is performed by one of processes selected from gas addition and ion-doping when said thin film is formed, and

said step of selectively doping is performed by an ion-doping process.

26. (Original) A method according to claim 25, wherein said ion-doping process is performed by using a non-mass separation type ion-doping apparatus having a DC filament ion source.

27. (Original) A method according to claim 23, wherein the concentration of p-type impurities in said thin film is adjusted to not more than $1 \times 10^{18}/cm^3$ by said step of non-selectively doping.

28. (Original) A CMOS device in which p- and n-type thin film transistors are formed, wherein

said p-type thin film transistor has a first active semiconductor layer formed by doping its channel region with p-type impurities at a concentration of not more than $1 \times 10^{18}/cm^3$ such that the concentration distribution in a direction of the thickness of said first active semiconductor layer is substantially uniform, and

said n-type thin film transistor has a second active semiconductor layer formed by doping its channel region with p-type impurities at a higher concentration than that in said first active semiconductor layer such that the concentration distribution in a direction of the thickness of said second active semiconductor layer has a peak near a surface.

29. (Original) A CMOS device in which p- and n-type thin film transistors are formed, wherein

said p-type thin film transistor has a first active semiconductor layer formed by doping its channel region with p-type impurities at a concentration of not more than 1x $10^{18}/cm^3$ such that the concentration distribution in a direction of the thickness of said first active semiconductor layer substantially changes broadly, and

said n-type thin film transistor has a second active semiconductor layer formed by doping its channel region with p-type impurities at a higher concentration than that in said first active semiconductor layer such that the concentration distribution in a direction of the thickness of said second active semiconductor layer has a peak near a surface.

30. (Currently Amended) A device according to claim 28, wherein each of said p- and n-type thin film transistors is formed such that the corresponding active semiconductor layer, a gate insulating film, and a gate electrode narrow down in this order, and provided with a source and a drain in said active semiconductor, said source and drain having LDD structures in accordance with ~~the~~ a difference in width between said active semiconductor layer, said gate insulating film and said gate electrode.

31. (Original) A device according to claim 28, wherein a gate electrode is formed by patterning under a gate insulating film below the source and drain of each of said thin film transistors.

32. (Currently Amended) An image display apparatus comprising:

an image display unit in which a plurality of pixels are arranged in a matrix;

a first control circuit for controlling the drive of rows of said image display unit; and

a second control circuit for controlling the drive of columns of said image display unit,

at least one of said image display unit and said first and second control circuits comprising a plurality of CMOS transistors in each of which p- and n-type thin film transistors are formed and which ~~have~~ are classified into at least two element groups having different operating voltages,

said p-type thin film transistor has a first active semiconductor layer formed by doping its channel region with p-type impurities such that the concentration distribution in a direction of the thickness of said first active semiconductor layer is substantially uniform, and

said n-type thin film transistor has a second active semiconductor layer formed by doping its channel region with p-type impurities at a higher concentration than that in said first active semiconductor layer such that the concentration distribution in a direction of the thickness of said second active semiconductor layer has a peak near a surface.

33. (Currently Amended) An image display apparatus comprising:

an image display unit in which a plurality of pixels are arranged in a matrix;

a first control circuit for controlling the drive of rows of said image display unit; and

a second control circuit for controlling the drive of columns of said image display unit,

at least one of said image display unit and said first and second control circuits comprising a plurality of CMOS transistors in each of which p- and n-type thin film transistors are formed and which ~~have~~ are classified into at least two element groups having different operating voltages,

said p-type thin film transistor has a first active semiconductor layer formed by doping its channel region with p-type impurities such that the concentration distribution in a direction of the thickness of said first active semiconductor layer substantially changes broadly, and

said n-type thin film transistor has a second active semiconductor layer formed by doping its channel region with p-type impurities at a higher concentration than that in said first active semiconductor layer such that the concentration distribution in a direction of the thickness of said second active semiconductor layer has a peak near a surface.

34. (Original) An apparatus according to claim 32, wherein the concentration of p-type impurities in said channel region of said p-type thin film transistor is not more than $1 \times 10^{18}/cm^3$.

35. (Original) An apparatus according to claim 32, wherein said image display unit has liquid crystal cells as said pixels and CMOS transistors with a high operating voltage, and

said first control circuit comprises a shift register having CMOS transistors with a relatively low operating voltage and an output buffer having CMOS transistors with a high operating voltage.